A DC to 38-GHz Distributed Analog Multiplier Using InP HEMT's

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***Abstract*— A novel distributed analog multiplier is proposed. It employs Gilbert cells as the unit section of the distributed structure. The single-ended analog multiplier MMIC's are built using 0.1-μm-gate-length InP HEMT's and uniplanar technology. The conversion gain is about −5 dB with LO power of 10 dBm. RF and IF 3-dB bandwidths are 38 and 16 GHz, respectively.**

I. Introduction

GILBERT-CELL-BASED analog multipliers are widely used as active double-balanced mixers in microwave applications (1). They are also the key components for high-bit-rate coherent optical heterodyne receivers in lightwave applications. Compared with conventional diode mixers, active mixers have advantages such as a positive conversion gain and good VSWR's for all ports. However, its wideband characteristics are severely limited by transistor performance. The best reported results are around 20 GHz, even when high-cutoff-frequency HBT devices are used [2], [3].

Distributed design is one way to obtain a wide bandwidth with less transistor-performance sensitivity. The use of a distributed structure for active FET mixers has already shown its advantages over conventional ones [4], [5]. However, previous works are only a simple extension of the distributed amplification concept because they used structures similar to distributed amplifiers. It is still questionable whether the distributed structure can be applied to more complicated circuits.

In this letter, we propose a new distributed analog multiplier using Gilbert cells as the unit sections. The MMIC's are fabricated using InP HEMT and uniplanar technolgy. They show a DC to 40-GHz bandwidth and demonstrate the design advance of the distributed structure for the analog multiplier.

II. Circuit Design

The distributed mixers reported so far have usually used single-gate common-source FET's or dual-gate common-source FET's as the unit sections. RF and LO signals are fed to the gate terminal while an IF signal is extracted from the drain terminal for the single-gate mixer. On the other hand, RF and LO signals are separately fed to the first and second gate terminals for the dual-gate mixer. Artificial transmission lines are formed at the gate and drain terminals by high-impedance transmission lines and time-averaged FET impedances.

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A distributed analog multiplier employs a completely different structure because the unit sections are Gilbert cells. Fig. 1 shows a schematic diagram of our 2-section distributed analog multiplier with a single-ended configuration. FET's $Q1$–$Q4$ form a Gilbert cell for the distributed-structure unit section. RF and LO signals are separately fed to the gate terminals of $Q3$ and $Q4$ while an IF signal is extracted from the drain terminal of $Q4$. RF and LO artificial transmission lines are formed by high-impedance transmission lines (T_{g1} and T_{g2}) and input impedances of $Q3$ and $Q4$. These artificial lines provide the wideband matching for the RF and LO signals. These lines are designed to have equal phase shifts between the unit sections as in conventional distributed mixers. An IF artificial transmission line is formed by a high-impedance transmission line (T_{d1}) and output impedance of $Q4$. The IF artificial line is necessary, especially for a up-converted signal. It is noteworthy that a small-signal input impedance can be used in the artificial-line design as it is in distributed-amplifier design. This is because FET's nonlinearity is not used, and it operates in the linear region for the analog multiplier. To insure the operation from DC frequency, the termination resistors (R_{gt} and R_{dt}) are directly connected to DC grounds. For the gate biases, a large resistor (R_{gb}) eliminates the effect of external inductances on the high-frequency performance. For the drain bias, a resistor-capacitor biasing network (R_{db}, R_{st} and C_{st}) is employed instead of a large resistor to reduce the supply voltage.

Detailed design was done with a harmonic balance simulator using a HEMT model with fT = 155 GHz and gm0= 1.4 S/mm. Gate widths of $Q1$ and $Q2$ are 200 μm, and $Q3$ and $Q4$ are 100 and 50 μm, respectively. The impedance of the high-impedance transmission line is 75 ohm. The designed performance is about a −8-dB conversion gain and a 50-GHz 3-dB RF bandwidth with a 0-dBm LO power and a 1-GHz IF frequency for the single-ended configuration shown in Fig. 1. Although the single-ended configuration is adopted in this work, a complete double-balanced mixer could be easily constructed in an MMIC format by using a passive balun or a distributed active balun.

III. Fabrication

MMIC's were fabricated using InAlAs/InGaAs/InP HEMT's with a gate length of 0.1 μm [6]. The transmission line is a coplanar waveguide. A microphotograph of an MMIC is shown in Fig. 2. Chip size is 2×2 mm.

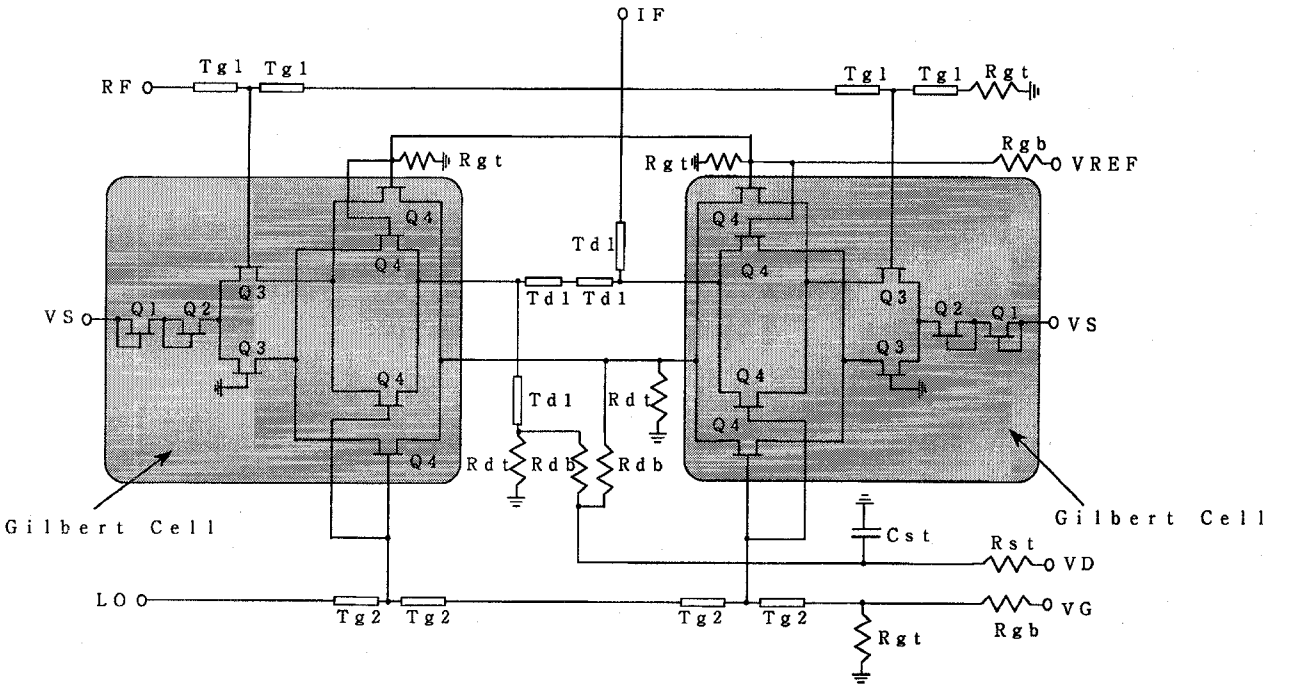

Fig. 1. Schematic diagram of the 2-section distributed analog multiplier with a single-ended configuration.

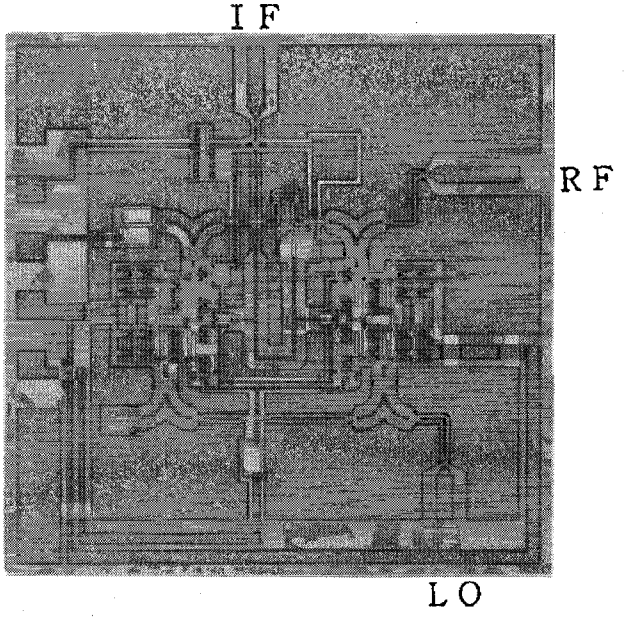

Fig. 2. Microphotograph of distributed analog multiplier MMIC.

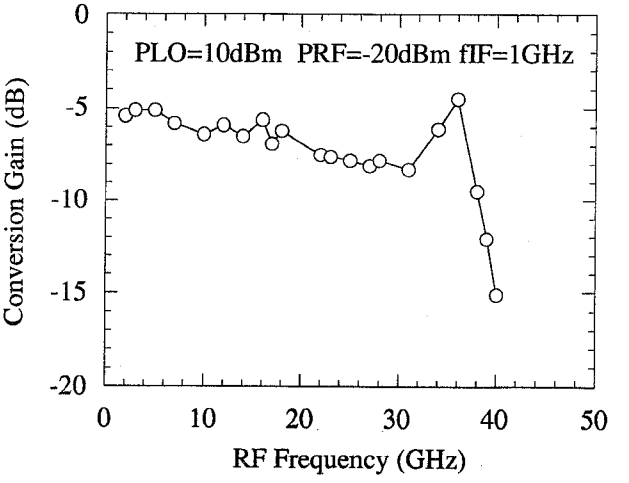

Fig. 3. Conversion gain as a function of RF frequency.

IV. Performance

MMIC's were measured using on-wafer probes. The conversion gain was measured at −20-dBm RF power. Fig. 3 shows the conversion gain as a function of RF frequency with IF frequency of 1 GHz and LO power of 10 dBm. The conversion gain was about −5 dB with a 3-dB RF bandwidth of about 38 GHz. DC power consumption was about 2.5 W. Fig. 4 shows the conversion gain versus the power level of LO power. IF and RF frequecies are 10 GHz and 1 GHz, respectively. The conversion gain almost saturated around 10 dBm of LO power. The conversion gain was lower than designed because the transconductance decreased more than expected. Fig. 5 shows the conversion gain as a function of IF frequency with LO frequency of 2 GHz and LO power of 10 dBm. The 3-dB IF bandwidth was about 16 GHz. RF and LO return losses were better than −10 dB in the frequency range below 30 GHz. Isolations were measured in RF and LO frequency ranges below 26 GHz. LO to RF isolation was better than 25 dB. RF to IF and LO to IF isolations were better than 10 dB. The conversion gain and isolations will be improved by using a double-balanced configuration. The decrease in bandwidth is larger than designed partly because of the extra transmission-line length. This layout restriction was caused by the relatively large area occupied by the unit sections. It will be avoided by reducing the device sizes. This also will reduce the total chip size.

V. Conclusion

A novel distribued analog multiplier has been proposed. It employs a Gilbert cell as the unit section of the distributed

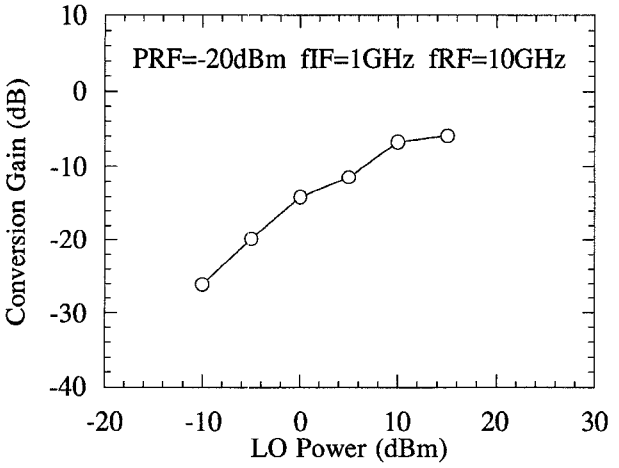

Fig. 4. Conversion gain as a function of LO power.

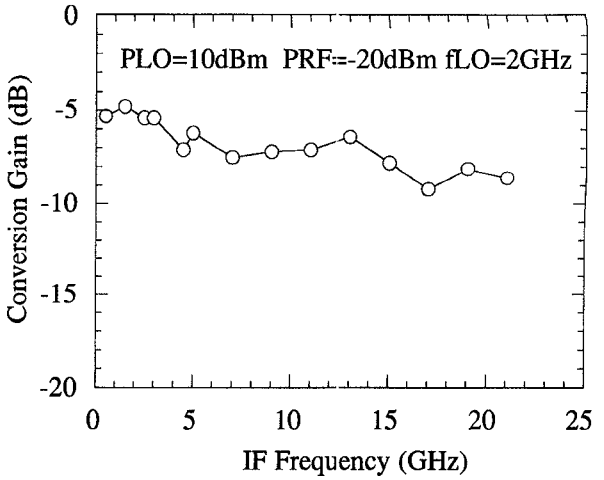

Fig. 5. Conversion gain as a function of IF frequency.

structure. Single-ended analog multiplier MMIC's were built using 0.1-μm-gate-length InP HEMT's and uniplanar technology. The conversion gain is about -5 dB with LO power of 10 dBm. RF and IF 3-dB bandwidths are 38 and 16 GHz, respectively. We believe these bandwidths are the widest ever reported for analog multipliers. Considering its impressive wideband performance, the proposed design technique should have a considerable impact on microwave and lightwave applications.

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